IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a first insulation layer formed on an inner surface of a trench formed in the semiconductor substrate and having its top located above the surface of the semiconductor substrate;

a diffusion layer formed within the semiconductor substrate, surrounding the deep portion of the trench;

a first conductive layer filled in the trench;

a gate electrode provided on a gate insulation layer formed on the surface of the semiconductor substrate;

source/drain diffusion layers formed in the surface of the semiconductor substrate, sandwiching a channel region below the gate electrode; ~~and~~

a second conductive layer extending on the first conductive layer, the first insulation layer, and one of the source/drain diffusion layers; and

a device isolation insulation layer having in its surface a concave whose bottom is located below a top of the first conductive layer.

2. (Original) The device according to claim 1, wherein the first insulation layer is provided on the inner surface of the trench without exposing a side of the semiconductor substrate within the trench.

3. (Original) The device according to claim 2, wherein the second conductive layer is provided without contacting the side of the semiconductor substrate.

4. (Original) The device according to claim 1, wherein a top of the first conductive layer is located above the surface of the semiconductor substrate.

5. (Original) The device according to claim 1, further comprising a second insulation layer overlying the top of the first insulation layer.

6. (Original) The device according to claim 1, further comprising a third insulation layer provided on the first conductive layer and consisting of a same material of the first insulation layer.

7. (Currently Amended) The device according to claim 6, ~~further comprising a~~ wherein the device isolation insulation layer ~~consisting~~ consists of a same material as the first and third insulation layers and ~~having in its surface a concave whose bottom~~ the bottom of the concave of the device isolation insulation layer is located above the surface of the semiconductor substrate.

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Previously Presented) The device according to claim 1, wherein an end of the one of the source/drain diffusion layers on which the second conductive layer extends contacts a side of the first insulation layer.

20. (Previously Presented) The device according to claim 1, wherein the second conductive layer electrically connects the first conductive layer to the one of the source/drain diffusion layers on which the second conductive layer extends.

21. (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a first insulation layer formed on an inner surface of a trench formed in the semiconductor substrate and having its top located above a surface of the semiconductor substrate;

a diffusion layer formed within the semiconductor substrate, surrounding the deep portion of the trench;

a first conductive layer filled in the trench;

a gate electrode provided on a gate insulation layer formed on the surface of the semiconductor substrate, a bottom surface of the gate electrode being lower than a top surface of the first conductive layer;

source/drain diffusion layers formed in the surface of the semiconductor substrate, sandwiching a channel region below the gate electrode; ~~and~~

a second conductive layer extending on the first conductive layer, the first insulation layer, and one of the source/drain diffusion layers; and

a device isolation insulation layer having in its surface a concave whose bottom is located below a top of the first conductive layer.

22. (Previously Presented) The device according to claim 21, wherein the first insulation layer is provided on the inner surface of the trench without exposing a side of the semiconductor substrate within the trench.

23. (Previously Presented) The device according to claim 22, wherein the second conductive layer is provided without contacting the side of the semiconductor substrate.

24. (Previously Presented) The device according to claim 21, wherein a top of the first conductive layer is located above the surface of the semiconductor substrate.

25. (Previously Presented) The device according to claim 21, further comprising a second insulation layer overlying the top of the first insulation layer.

26. (Previously Presented) The device according to claim 21, further comprising a third insulation layer provided on the first conductive layer and consisting of a same material of the first insulation layer.

27. (Currently Amended) The device according to claim 26, ~~further comprising a~~ wherein the device isolation insulation layer ~~consisting~~ consists of a same material as the first and third insulation layers and ~~having in its surface a concave whose~~ the bottom of the

concave of the device isolation insulation layer is located above the surface of the semiconductor substrate.

28. (Previously Presented) The device according to claim 21, wherein an end of the one of the source/drain diffusion layers on which the second conductive layer extends contacts a side of the first insulation layer.

29. (Previously Presented) The device according to claim 21, wherein the second conductive layer electrically connects the first conductive layer to the one of the source/drain diffusion layers on which the second conductive layer extends.

30. (New) The device according to claim 1, further comprising a dummy gate electrode provided above the device isolation insulation layer and having a thickness thinner than that of the gate electrode.

31. (New) The device according to claim 21, further comprising a dummy gate electrode provided above the device isolation insulation layer and having a thickness thinner than that of the gate electrode.